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UNITRODE

APPLICATION NOTE

UC3842/3/4/5 PROVIDES LOW-COSTCURRENT-MODE CONTROL

INTRODUCTION

U-100A

The fundamental challenge of power supply design is to simultaneously realize two conflicting objectives: good electrical performance and low cost. The UC3842/3/4/5 is an integrated pulse width modulator (PWM) designed with both these objectives in mind. This IC provides designers an inexpensive controller with which they can obtain all the performance advantages of current mode operation. In addition, the UC3842 series is optimized for efficient power sequencing of off-line converters, DC to DC regulators and for driving power MOSFETs or transistors.

This application note provides a functional description of the UC3842 family and highlights the features of each individual member, the UC3842, UC3843, UC3844 and UC3845 Throughout the text, the UC3842 part number will be referenced, however the generalized circuits and performance characteristics apply to each member of the UC3842 series unless otherwise noted. A review of current mode control and its benefits is included and methods of avoiding common pitfalls are mentioned. The final section presents designs of power supplies utilizing UC3842 control.

CURRENT-MODE CONTROL

Figure 1 shows the two-loop current-mode control system in a typical buck regulator application. A clock signal initiates power pulses at a fixed frequency. The termination of each pulse occurs when an analog of the inductor current reaches a threshold established by the error signal. In this way the error signal actually controls peak inductor current. This contrasts with conventional schemes in which the error signal directly controls pulse width without regard to inductor current.

Several performance advantages result from the use of current-mode control. First, an input voltage feed-forward characteristic is achieved; i.e., the control circuit instantaneously corrects for input voltage variations without using up any of the error amplifier's dynamic range. Therefore, line regulation is excellent and the error amplifier can be dedicated to correcting for load variations exclusively.

For converters in which inductor current is continuous, controlling peak current is nearly equivalent to controlling average current. Therefore, when such converters employ current-mode control, the inductor can be treated as an

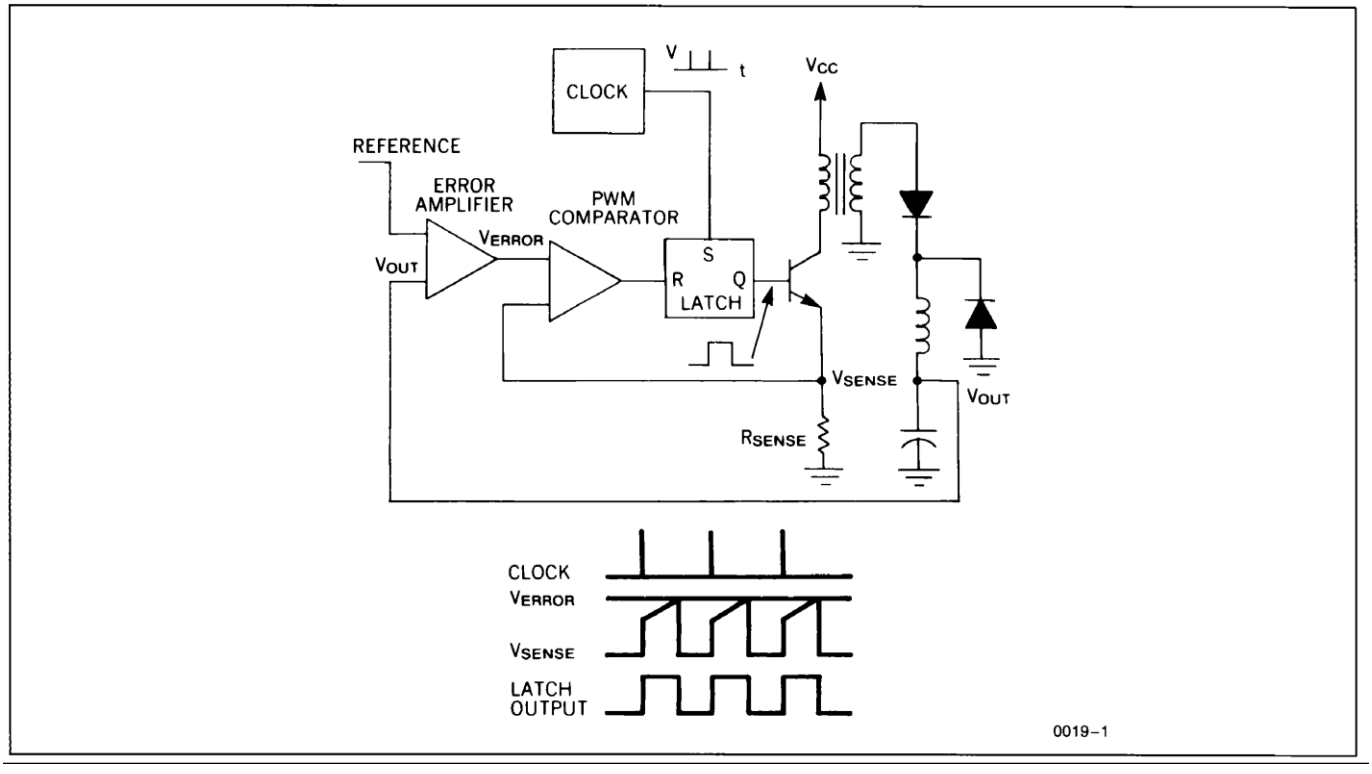


Figure 1. Two-Loop Current-Mode Control System

error-voltage-controlled-current-source for the purposes of small-signal analysis. This is illustrated by Figure 2. The two-pole control-to-output frequency response of these converters is reduced to a single-pole (filter capacitor in parallel with load) response. One result is that the error amplifier compensation can be designed to yield a stable closed-loop converter response with greater gainbandwidth than would be possible with pulse-width control, giving the supply improved small-signal dynamic response to changing loads. A second result is that the error amplifier compensation circuit becomes simpler, as illustrated in Figure 3. Capacitor C_i and resistor R_{iz} in Figure 3a add a low frequency zero which cancels one of the two control-to-output poles of non-current-mode converters. For large-signal load changes, in which converter response is limited by inductor slew rate, the error amplifier will saturate while the inductor is catching up with the load. During this time, C_f will charge to an abnormal level. When the inductor current reaches its required level, the voltage on C_f causes a corresponding error in supply output voltage. The recovery time is $R_f C_f$ which may be quite long. However, the compensation network of Figure 3b can be used where current-mode control has eliminated the inductor pole. Large-signal dynamic response is then greatly improved due to the absence of C_f.

Current limiting is greatly simplified with current-mode control. Pulse-by-pulse limiting is, of course, inherent in the control scheme. Furthermore, an upper limit on the peak current can be established by simply clamping the error voltage. Accurate current limiting allows optimization of magnetic and power semiconductor elements while ensuring reliable supply operation.

Finally, current-mode controlled power stages can be operated in parallel with equal current sharing. This opens the possibility of a modular approach to power supply design.

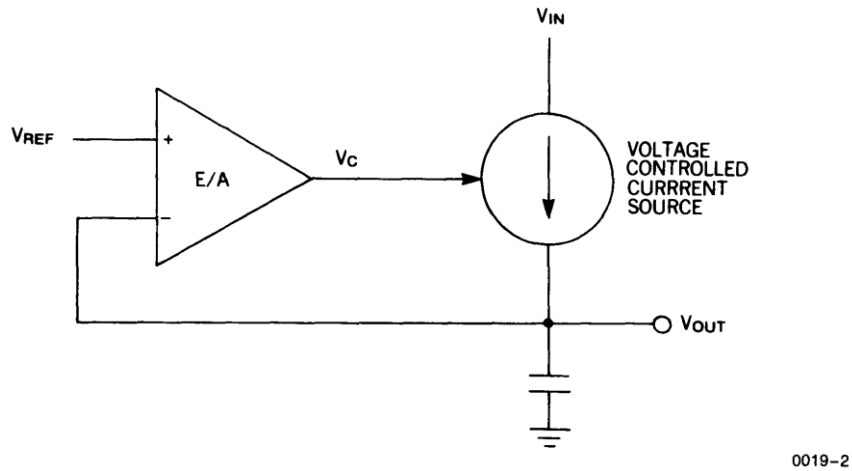
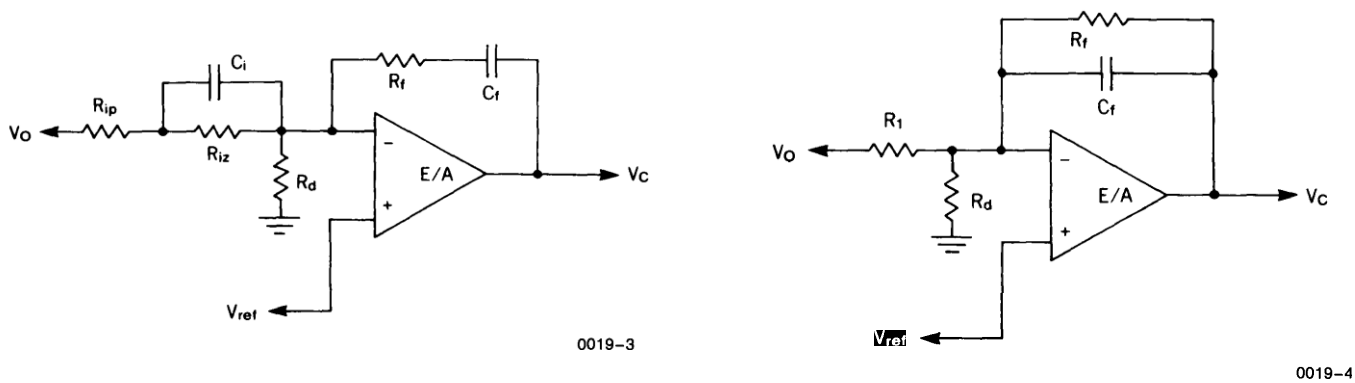


Figure 2. Inductor Looks Like a Current Source to Small Signals



A) Direct Duty Cycle Control **B) Current Mode Control**

Figure 3. Required Error Amplifier Compensation for Continuous Inductor Current Designs

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THE UC3842/3/4/5 SERIES OF CURRENT-MODE PWM IC'S

DESCRIPTION

The UC1842/3/4/5 family of control ICs provides the necessary features to implement off-line or DC to DC fixed frequency current mode control schemes with a minimal external parts count. Internally implemented circuits include under-voltage lockout featuring start up current less than 1 mA, a precision reference trimmed for accuracy at the error amp input, logic to insure latched operation, a PWM comparator which also provides current limit control, and a totem pole output stage designed to source or sink high peak current. The output stage, suitable for driving either N Channel MOSFETs or bipolar transistor switches, is low in the off state.

Differences between members of this family are the under-voltage lockout thresholds and maximum duty cycle ranges. The UC1842 and UC1844 have UVLO thresholds of 16V (on) and 10V (off), ideally suited to off-line applications. The corresponding thresholds for the UC1843 and UC1845 are 8.5V and 7.9V. The UC1842 and UC1843 can operate to duty cycles approaching 100%. A range of zero to <50% is obtained by the UC1844 and UC1845 by the addition of an internal toggle flip flip which blanks the output off every other clock cycle.

FEATURES

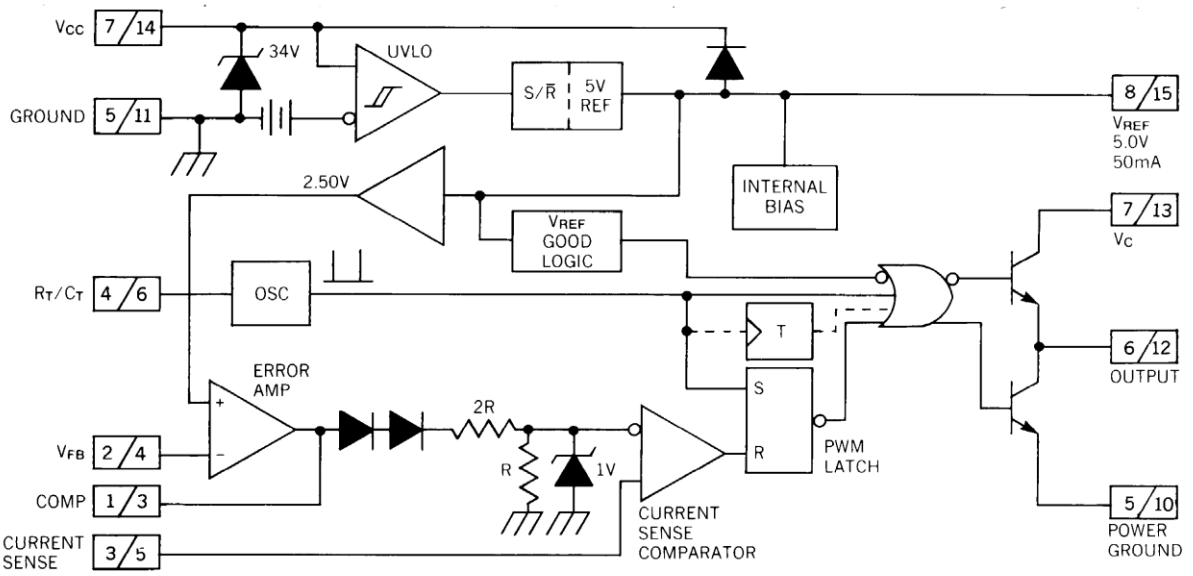
- Optimized for Off-Line and DC to DC Converters
- Low Start Up Current (< 1 mA)
- Automatic Feed Forward Compensation
- Pulse-By-Pulse Current Limiting
- Enhanced Load Response Characteristics
- Under-Voltage Lockout with Hysteresis
- Double Pulse Suppression
- High Current Totem Pole Output
- Internally Trimmed Bandgap Reference
- 500 kHz Operation
- Low R_O Error Amp

IC SELECTION GUIDE

UVLO START	MAXIMUM DUTY CYCLE	
	<50%	<100%
8.5V	UC3845	UC3843
16V	UC3844	UC3842

RECOMMENDED USAGE

APPLICATION (CIRCUIT)	POWER SUPPLY INPUT (V)	
	HIGH (OFFLINE)	LOW (DC/DC)
FLYBACK	UC3844	UC3845
FORWARD	UC3844/2	UC3845/3
BUCK/BOOST	UC3842/4	UC3843/5



Note: 1. A/B A= DIL-8 Pin Number. B = SO-16 Pin Number.
2. Toggle flip flop used only in 1844A and 1845A.

Figure 4

UNDER-VOLTAGE LOCKOUT

The UVLO circuit insures that V_{CC} is adequate to make the UC3842/3/4/5 fully operational before enabling the output stage. Figure 5 shows that the UVLO turn-on and turn-off thresholds are fixed internally at 16V and 10V respectively. The 6V hysteresis prevents V_{CC} oscillations during power sequencing. Figure 6 shows supply current requirements. Start-up current is less than 1 mA for efficient bootstrapping from the rectified input of an off-line converter, as illustrated by Figure 6. During normal circuit operation, V_{CC} is developed from auxiliary winding W_{AUX} with D_1 and C_{IN}. At start-up, however, C_{IN} must be charged to 16V through R_{IN}. With a start-up current of 1 mA, R_{IN} can be as large as 100 kΩ and still charge GIN when V_{AC} = 90V RMS (low line). Power dissipation in R_{IN} would then be less than 350 mW even under high line (V_{AC} = 130V RMS) conditions.

During UVLO; the output driver is in a low state. While it doesn't exhibit the same saturation characteristics as normal operation, it can easily sink 1 milliamp, enough to insure the MOSFET is held off.

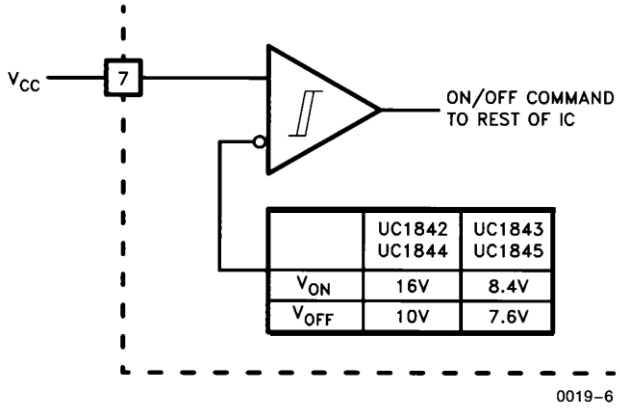


Figure 5

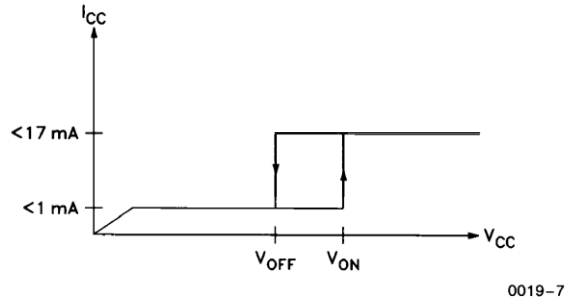


Figure 6. During Under-Voltage Lockout, the output driver is biased to sink minor amounts of current.

OSCILLATOR

The UC3842 oscillator is programmed as shown in Figure 8. Timing capacitor CT is charged from V_{REF} (5V) through the timing resistor R_T and discharged by an internal current source.

The first step in selecting the oscillator components is to determine the required circuit deadtime. Once obtained, Figure 9 is used to pinpoint the nearest standard value of CT for a given deadtime. Next, the appropriate R_T value is interpolated using the parameters for C_T and oscillator frequency. Figure 10 illustrates the R_T/C_T combinations versus oscillator frequency. The timing resistor can be calculated from the following formula.

$$F_{OSC}\ (kHz) = 1.72\ /\ (R_T\ (k) \times C_T\ (\mu f))$$

The UC3844 and UC3845 have an internal divide-by-two flip-flop driven by the oscillator for a 50% maximum duty cycle. Therefore, their oscillators must be set to run at twice the desired power supply switching frequency. The UC3842 and UC3843 oscillator runs AT the switching frequency. Each oscillator of the UC3842/3/4/5 family can be used to a maximum of 500 kHz.

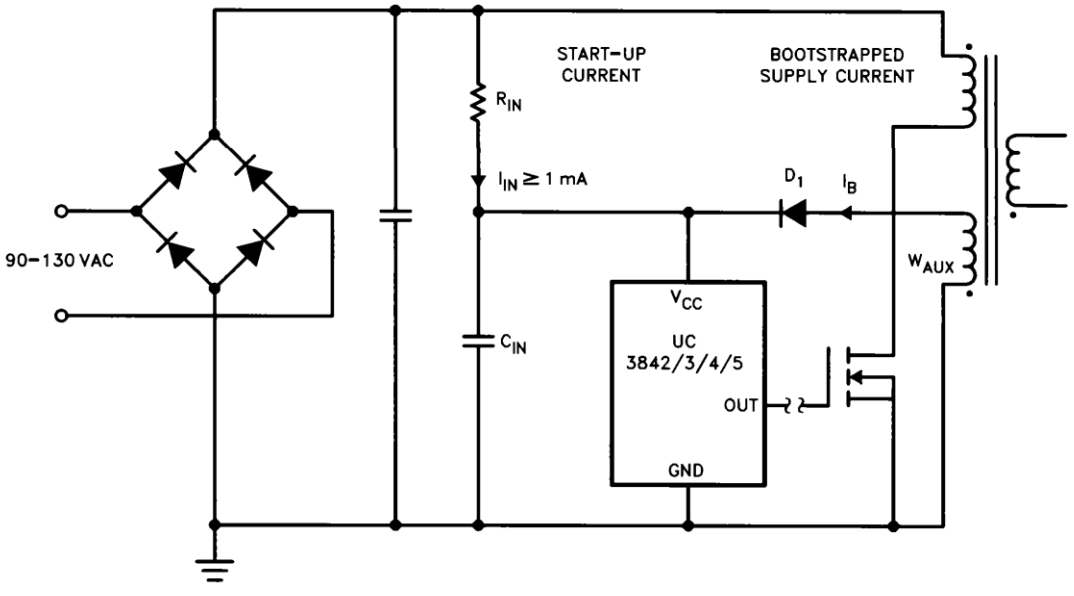


Figure 7. Providing Power to the UC3842/3/4/5

MAXIMUM DUTY CYCLE

The UC3842 and UC3843 have a maximum duty cycle of approximately 100%, whereas the UC3844 and UC3845 are clamped to 50% maximum by an internal toggle flip flop. This duty cycle clamp is advantageous in most flyback and forward converters. For optimum IC performance the deadtime should not exceed 15% of the oscillator clock period.

During the discharge, or "dead" time, the internal clock signal blanks the output to the low state. This limits the maximum duty cycle D_{MAX} to:

$D_{MAX} = 1 - (t_{DEAD} / t_{PERIOD})$ UC3842/3

$D_{MAX} = 1 - (t_{DEAD} / 2 \times t_{PERIOD})$ UC3844/5

where $T_{PERIOD} = 1 / F$ oscillator

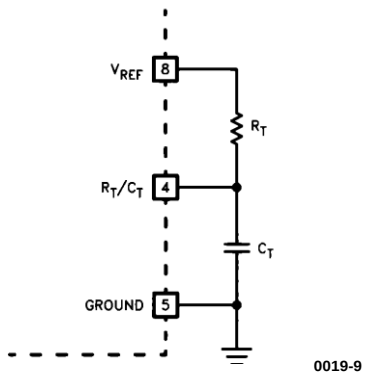


Figure 8

Deadtime vs C_T (R_T > 5k)

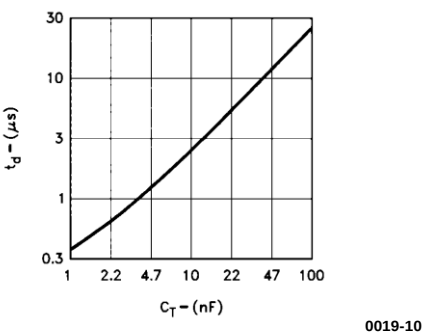


Figure 9

Timing Resistance vs Frequency

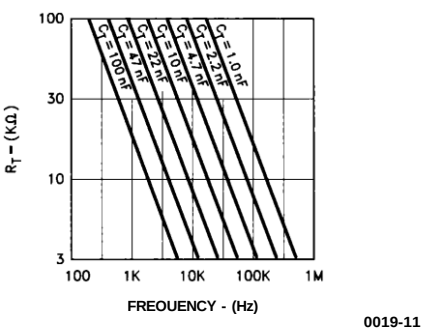


Figure 10

CURRENT SENSING AND LIMITING

The UC3842 current sense input is configured as shown in Figure 12. Current-to-voltage conversion is done externally with ground-referenced resistor R_S. Under normal operation the peak voltage across R_S is controlled by the E/A according to the following relation:

$$I_P = \frac{V_C - 1.4V}{3\,R_S}$$

where V_C = control voltage = E/A output voltage.

R_S can be connected to the power circuit directly or through a current transformer, as Figure 11 illustrates. While a direct connection is simpler, a transformer can reduce power dissipation in R_S, reduce errors caused by the base current, and provide level shifting to eliminate the restraint of ground-referenced sensing. The relation between V_C and peak current in the power stage is given by:

$$i_{(pk)} = N\left(\frac{V_{RS(pk)}}{R_S}\right) = \frac{N}{3\,R_S}\left(V_C - 1.4V\right)$$

where: N = current sense transformer turns ratio
= 1 when transformer not used.

For purposes of small-signal analysis, the control-to-sensed-current gain is:

$$\frac{i_{(pk)}}{V_C} = \frac{N}{3\,R_S}$$

When sensing current in series with the power transistor, as shown in Figure 11, the current waveform will often have a large spike at its leading edge. This is due to rectifier recovery and/or inter-winding capacitance in the power transformer. If unattenuated, this transient can prematurely terminate the output pulse. As shown, a simple RC filter is usually adequate to suppress this spike. The RC time constant should be approximately equal to the current spike duration (usually a few hundred nanoseconds).

The inverting input to the UC3842 current-sense comparator is internally clamped to 1V (Figure 12). Current limiting occurs if the voltage at pin 3 reaches this threshold value, i.e., the current limit is defined by:

$$i_{max} = \frac{N \times 1V}{R_s}$$

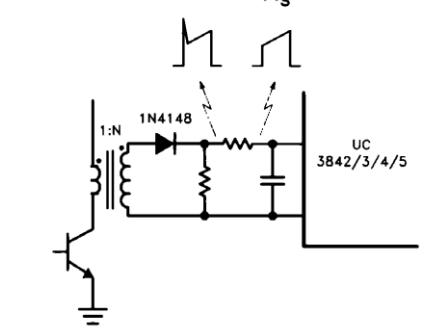


Figure 11. Transformer-Coupled Current Sensing

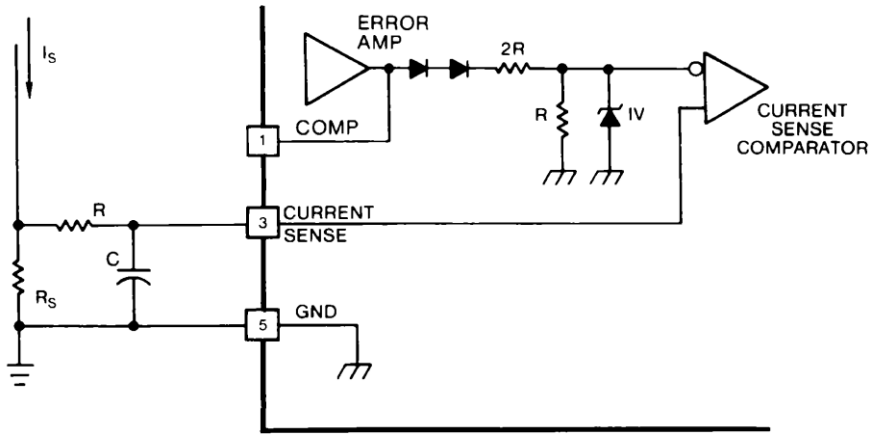


Figure 12. Current Sensing

ERROR AMPLIFIER

The error amplifier (E/A) configuration is shown in Figure 13. The non-inverting input is not brought out to a pin, but is internally biased to 2.5V ± 2%. The E/A output is available at pin 1 for external compensation, allowing the user to control the converter's closed-loop frequency response.

Figure 14 shows an E/A compensation circuit suitable for stabilizing any current-mode controlled topology except for flyback and boost converters operating with inductor current. The feedback components add a pole to the loop transfer function at $f_P = 1/2\pi R_F C_F$. R_F and C_F are chosen so that this pole cancels the zero of the output filter capacitor ESR in the power circuit. R_I and R_F fix the low-frequency gain. They are chosen to provide as much gain as possible while still allowing the pole formed by the output filter capacitor and load to roll off the loop gain to unity (0 dB) at $f \approx f_{SWITCHING}/4$. This technique insures converter stability while providing good dynamic response.

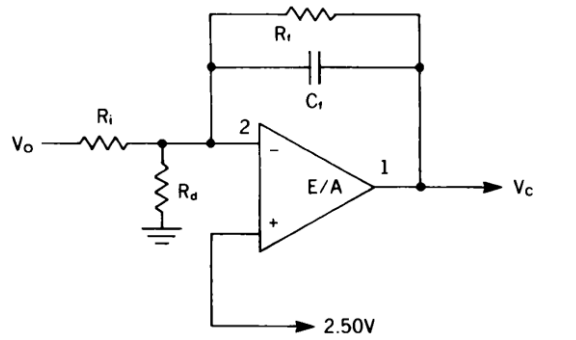


Figure 14. Compensation

The E/A output will source 0.5 mA amd sink 2 mA. A lower limit for R_F is given by:

$$R_{F(MIN)} \approx \frac{V_{EA\ OUT\ (MAX)} - 2.5V}{0.5\ mA} = \frac{6V - 2.5V}{0.5\ mA} = 7\ k\Omega.$$

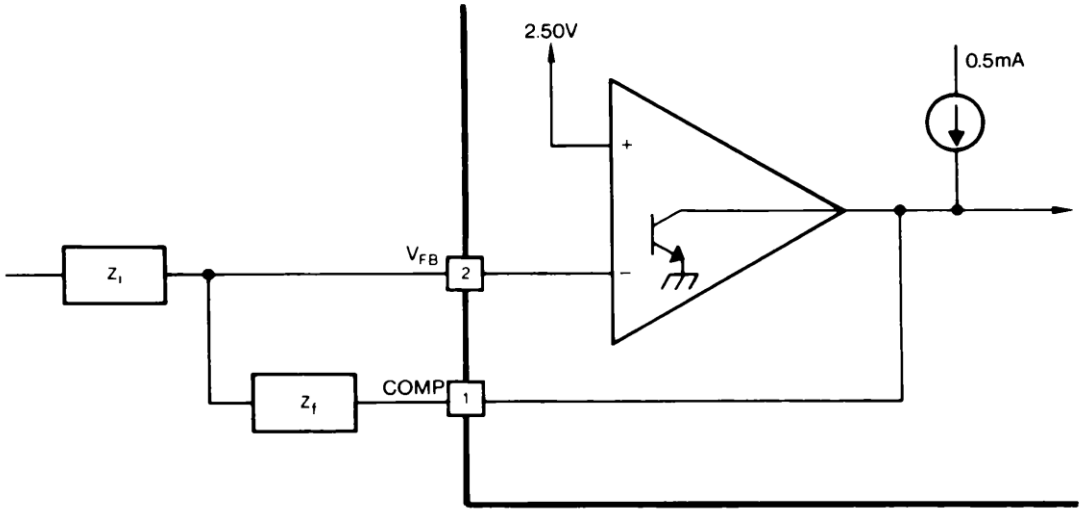


Figure 13. E/A Configuration

E/A input bias curret (2 μA max) flows through R_I resulting in a DC error in output voltage (V_O) given by:

$$\Delta V_{O(MAX)} = (2\ \mu A)\ R_I,$$

It is therefore desirable to keep the value of R_I as low as possible.

Figure 15 shows the open-loop frequency response of the UC3842 E/A. The gain represents an upper limit on the gain of the compensated E/A. Phase lag increases rapidly as frequency exceeds 1 MHz due to second-order poles at ~ 10 MHz and above.

Continuous-inductor-current boost and flyback converters each have a right-half-plane zero in their transfer function. An additional compensation pole is needed to roll off loop gain at a frequency less than that of the RHP zero. R_P and C_P in the circuit of Figure 16 provide this pole.

TOTEM-POLE OUTPUT

The UC3842 PWM has a single totem-pole output which can be operated to ± 1 amp peak for driving MOSFET gates, and a + 200 mA average current for bipolar power transistors. Cross conduction between the output transistors is minimal, the average added power with V_{IN} = 30V is only 80 mW at 200 kHz.

Limiting the peak current through the IC is accomplished by placing a resistor between the totem-pole output and the gate of the MOSFET. The value is determined by dividing the totem-pole collector voltage V_C by the peak current rating of the IC's totem-pole. Without this resistor, the peak current is limited only by the dV/dT rate of the totem-pole switching and the FET gate capacitance.

The use of a Schottky diode from the PWM output to ground will prevent the output voltage from going excessively below ground, causing instabilities within the IC. To be effective, the diode selected should have a forward drop of less than 0.3V at 200 mA. Most l- to 3-amp Schottky diodes exhibit these traits above room temperature. Placing the diode as physically close to the PWM as possible will enhance circuit performance. Implementation of the complete drive scheme is shown in the following diagrams. Transformer driven circuits also require the use of the Schottky diodes to prevent a similar set of circum-

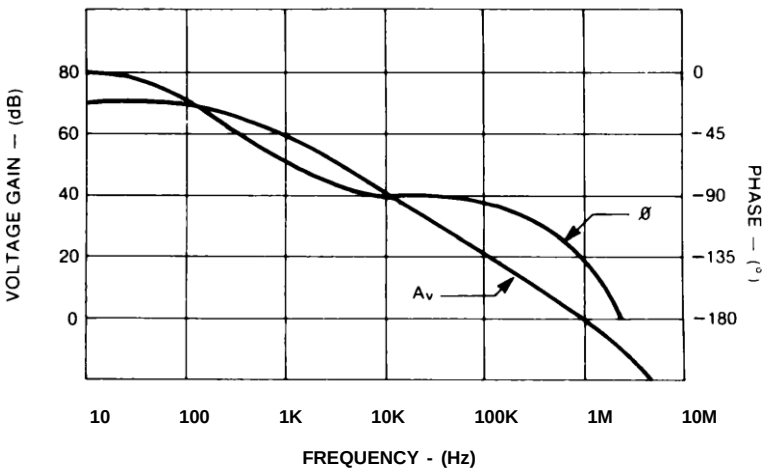


Figure 15. Error Amplifier Open-Loop Frequency Response

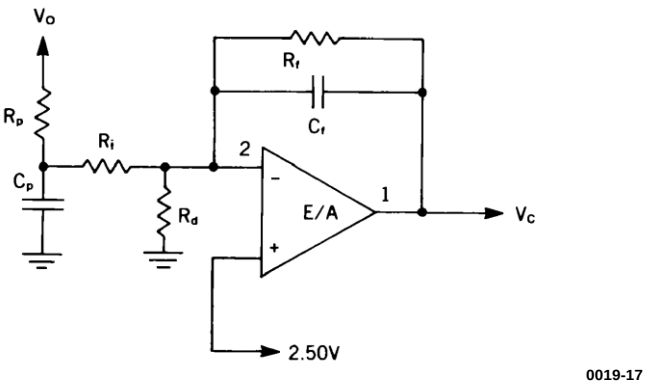


Figure 16. E/A Compensation Circuit for Continuous Boost and Flyback Topologies

stances from occurring on the PWM output. The ringing below ground is greatly enhanced by the transformer leakage inductance and parasitic capacitance, in addition to the magnetizing inductance and FET gate capacitance. Circuit implementation is similar to the previous example.

Figures 18, 19 and 20 show suggested circuits for driving MOSFETs and bipolar transistors with the UC3842 output. The simple circuit of Figure 18 can be used when the control IC is not electrically isolated from the MOSFET turn-on and turn-off to ± 1 amp. It also provides damping for a parasitic tank circuit formed by the FET input capacitance and series wiring inductance. Schottky diode D1 prevents the output of the IC from going far below ground during turn-off.

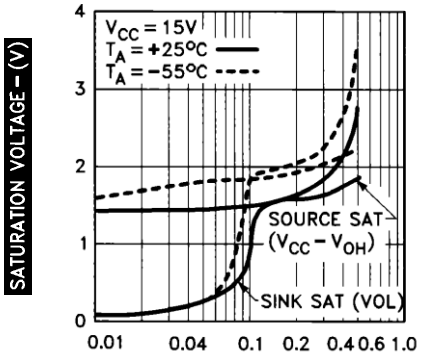


Figure 17. Output Saturation Characteristics

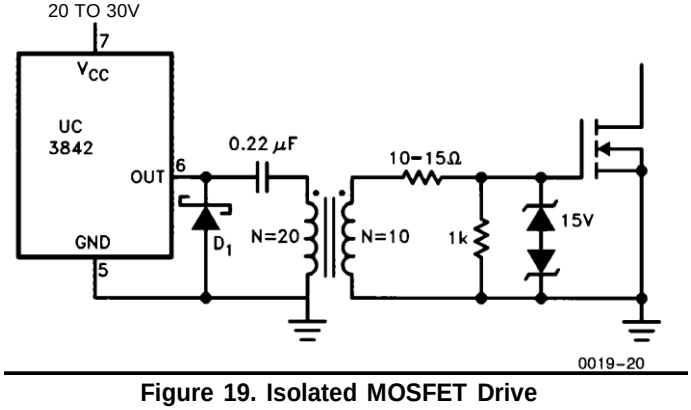


Figure 19. Isolated MOSFET Drive

Figure 19 shows an isolated MOSFET drive circuit which is appropriate when the drive signal must be level shifted or transmitted across an isolation boundary. Bipolar transistors can be driven efficiently with the circuit of Figure 20. Resistors R_1 and R_2 fix the on-state base current while capacitor C_1 provides a negative base current pulse to remove stored charge at turn-off.

Since the UC3842 series has only a single output, an interface circuit is needed to control push-pull half or full bridge topologies. The UC3706 dual output driver with internal toggle flip-flop performs this function. A circuit example at the end of this paper illustrates a typical application for these two ICs. Increased drive capability for driving numerous FETs in parallel, or other loads can be accomplished using one of the UC3705/6/7 driver ICs.

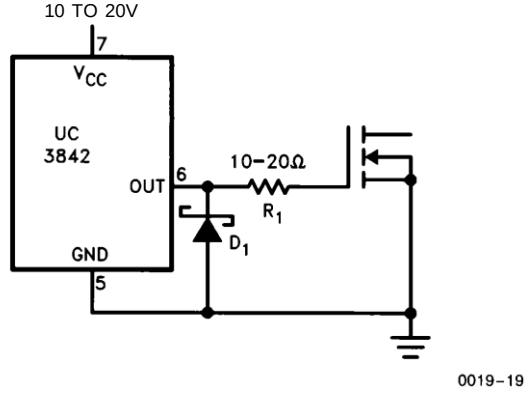


Figure 18. Direct MOSFET Drive

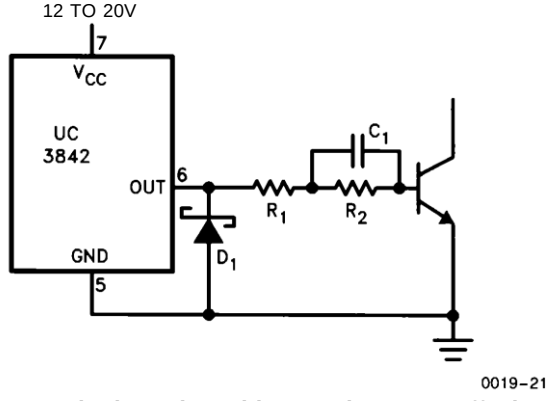


Figure 20. Bipolar Drive with Negative Turn-Off Bias

NOISE

As mentioned earlier, noise on the current sense or control signals can cause significant pulse-width jitter, particularly with continuous-inductor-current designs. While slope compensation helps alleviate this problem, a better solution is to minimize the amount of noise. In general, noise immunity improves as impedances decrease at critical points in a circuit.

One such point for a switching supply is the ground line. Small wiring inductances between various ground points on a PC board can support common-mode noise with sufficient amplitude to interfere with correct operation of the modulating IC. A copper ground plane and separate return lines for high-current paths greatly reduce common-mode noise. Note that the UC3842 has a single ground pin. High sink currents in the output therefore cannot be returned separately.

Ceramic monolythic bypass capacitors (0.1 μF) from V_{CC} and V_{REF} to ground will provide low-impedance paths for high frequency transients at those points. The input to the error amplifier, however, is a high-impedance point which cannot be bypassed without affecting the dynamic response of the power supply. Therefore, care should be taken to lay out the board in such a way that the feedback path is far removed from noise generating components such as the power transistor(s).

Figure 21 illustrates another common noise-induced problem. When the power transistor turns off, a noise spike is coupled to the oscillator R_T/C_T terminal. At high duty cycles the voltage at R_T/C_T is approaching its threshold level (~ 2.7V, established by the internal oscillator circuit) when this spike occurs. A spike of sufficient amplitude will prematurely trip the oscillator as shown by the dashed lines. In order to minimize the noise spike, choose C_T as large as possible, remembering that deadtime increases with C_T. It is recommended that C_T never be less than ~ 1000 pF. Often the noise which causes this problem is caused by the output (pin 6) being pulled below ground at turn-off by external parasitics. This is particularly true when driving MOSFETs. A Schottky diode clamp from ground to pin 6 will prevent such output noise from feeding to the oscillator. If these measures fail to correct the probelm, the oscillator frequency can always be stabilized with an external clock. Using the circuit of Figure 31 results in an R_T/C_T waveform like that of Figure 21B. Here the oscillator is much more immune to noise because the ramp voltage never closely approaches the internal threshold.

SYNCHRONIZATION

The simplest method to force synchronization utilizes the timing capacitor (C_T) in near standard configuration. Rather than bring C_T to ground directly, a small resistor is placed in series with C_T to ground. This resistor serves as the input for the sync pulse which raises the C_T voltage above the oscillator's internal upper threshold. The PWM is allowed to run at the frequency set by R_T and C_T until the sync pulse appears. This scheme offers several advantages including having the local ramp available for slope compensation. The UC3842/3/4/5 oscillator

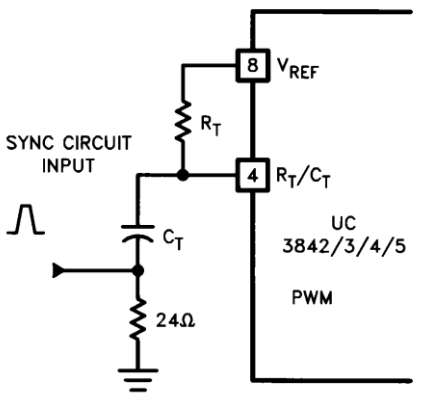


Figure 22. Sync Circuit Implementation

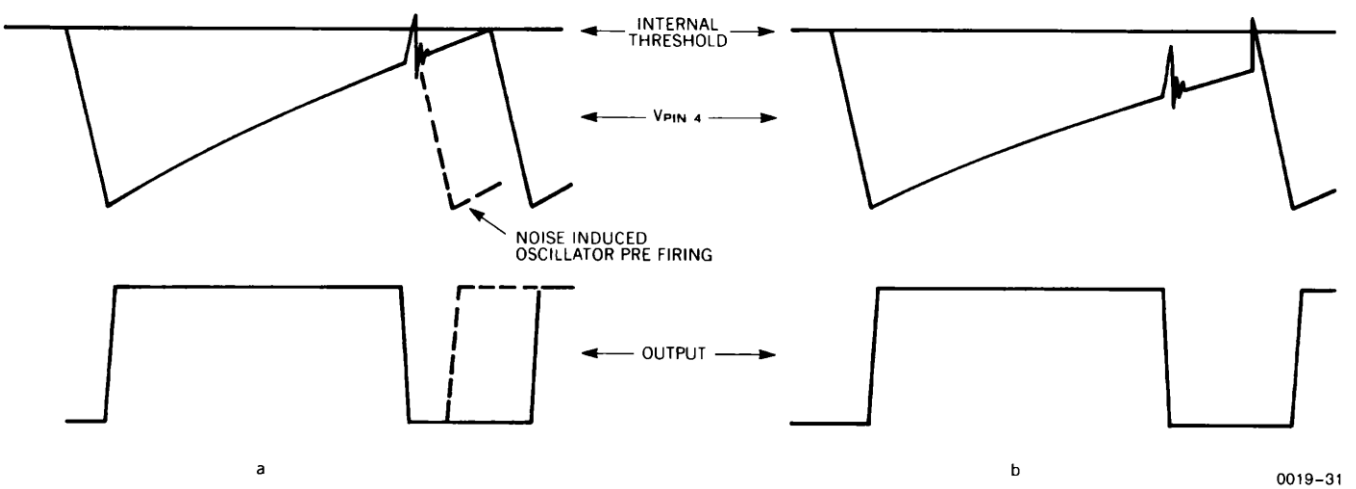


Figure 21. (a.) Noise on Pin 4 can cause oscillator to pre-trigger.
(b.) With external sync., noise does not approach threshold level.

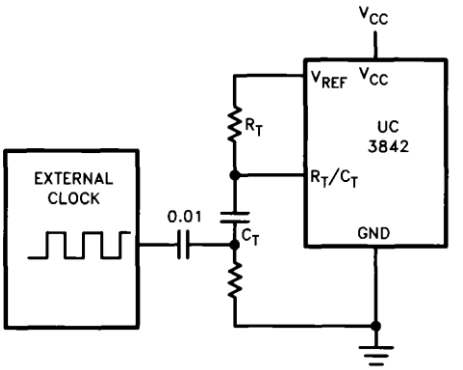
must be set to a lower frequency than the sync pulse stream, typically 20 percent with a 0.5V pulse applied across the resistor. Further information on synchronization can be found in “Practical Considerations in Current Mode Power Supplies” listed in the reference appendix.

The UC3842 can also be synchronized to an external clock source through the R_T/C_T terminal (Pin 4) as shown in Figure 23.

In normal operation, the timing capacitor C_T is charged between two thresholds, the upper and lower comparator limits. As C_T begins its charge cycle, the output of the PWM is initiated and turns on. The timing capacitor continues to charge until it reaches the upper threshold of the internal comparator. Once intersected, the discharge circuitry activates and discharges C_T until the lower threshold is reached. During this discharge time the PWM output is disabled, thus insuring a “dead” or off time for the output.

A digital representation of the oscillator charge/discharge status can be utilized as an input to the R_T/C_T terminal. In instances like this, where no synchronization port is easily available, the timing circuitry can be driven from a digital logic input rather than the conventional analog mode. The primary considerations of on-time, dead-time, duty cycle and frequency can be encompassed in the digital pulse train input.

A LOW logic level input determines the PWM maximum ON time. Conversely, a HIGH input governs the OFF, or dead time. Critical constraints of frequency, duty cycle or dead time can be acurately controlled by anything from a 555 timer to an elaborate microprocessor controlled software routine.



$D_{Max} = t_L\ (t_H + t_L)$
$t_H = 0.693\ (R_A + R_B)\ C$
$t_L = 0.693\ R_B C$

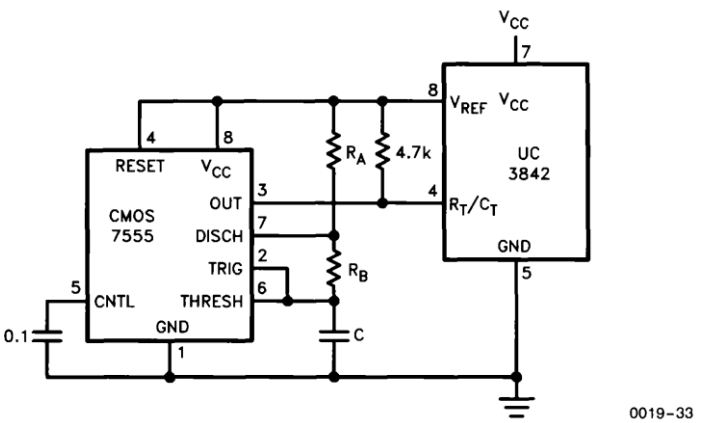


Figure 23

Synchronization to an External Clock

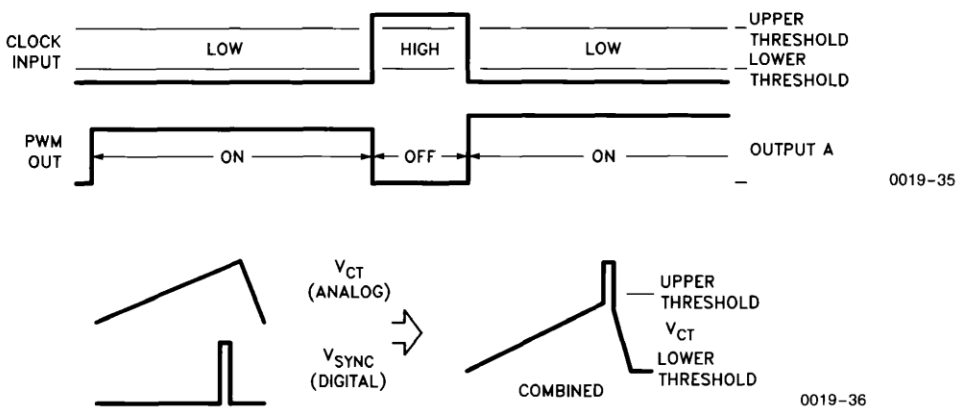


Figure 24

SYNC PULSE GENERATOR

The UC3842/3/4/5 oscillator can be used to generate sync pulses with a minimum of external components. This simple circuit shown in Figure 25 triggers on the falling edge of the C_T waveform, and generates the sync pulse required for the previously mentioned synchronization scheme. Triggered by the master's deadtime, this circuit is **useable to several hundred kilohertz with a minimum of** delays between the master and slave(s). The photos shown in Figures 26 and 27 depict the circuit waveforms of interest.

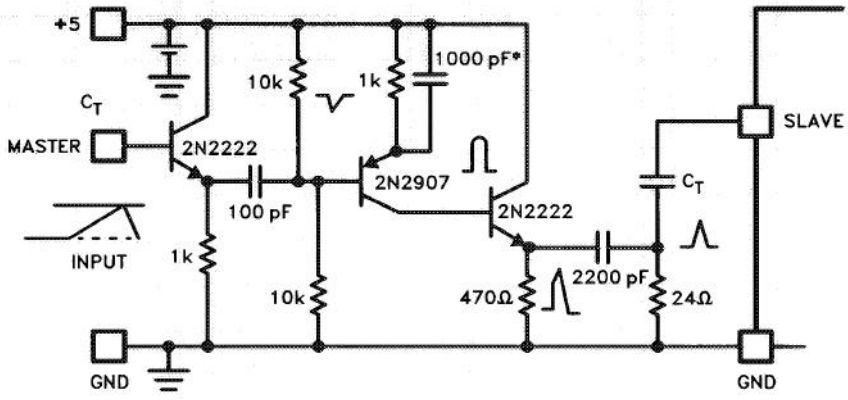


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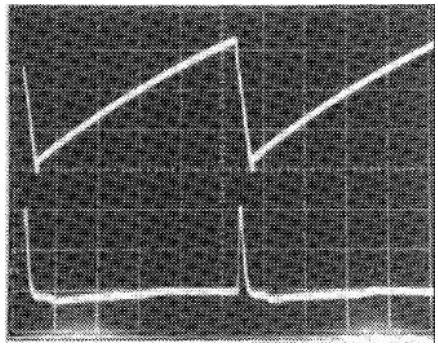
Figure 25. Sync Pulse Generator Circuit



Top Trace:
Circuit Input

Bottom Trace:
Circuit Output
Across 24 Ohms

Vertical: O.5V/CM Both
Horizontal: 0.5μS/CM

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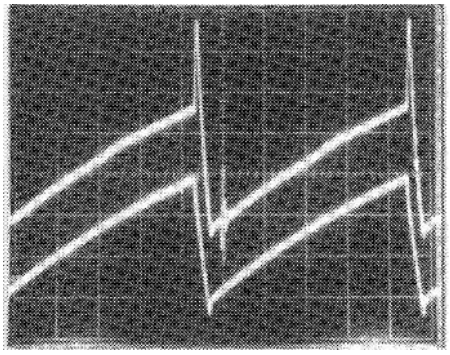
Figure 26. Operating Waveforms at 500 kHz



Top Trace:
Slave C_T

Bottom Trace:
Master C_T

Vertical: 0.5V/CM Both
Horizontal:0.5μS/CM

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Figure 27. Master/Slave Sync Waveforms at C_T

CHARGE PUMP CIRCUITS
LOW POWER DC/DC CONVERSION

Step Up
$V_O \approx 2 \times V_{IN}$

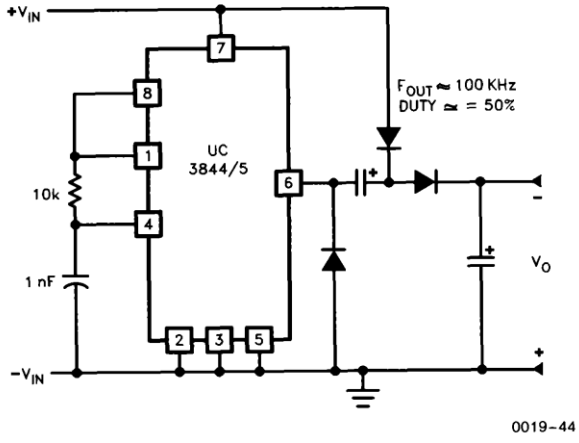

Figure 28

Inverting
$V_O \approx -V_{IN}$

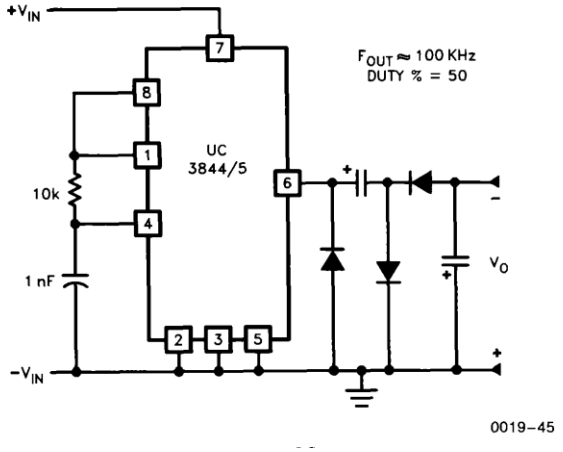

Figure 29

Low Power Buck Regulator-Voltage Mode

The basic buck regulator is described in the UNITRODE Applications Handbook.

*Consult UNITRODE Power Supply Design Seminar Book for compensation details; see “Closing The Feedback Loop”, Buck Topology.

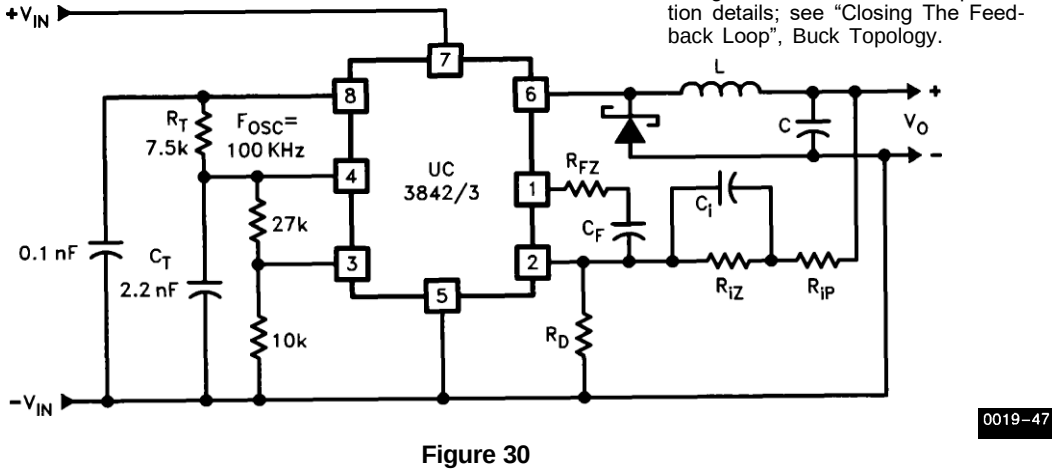

Figure 30

CIRCUIT EXAMPLES

1. Off-Line Flyback

Figure 31 shows a 25W multiple-output off-line flyback regulator controlled with the UC3844. This regulator is low in cost because it uses only two magnetic elements, a primary-side voltage sensing technique, and an inexpensive control circuit. Specifications are listed below.

Also consult UNITRODE application note U-96 in the applications handbook.

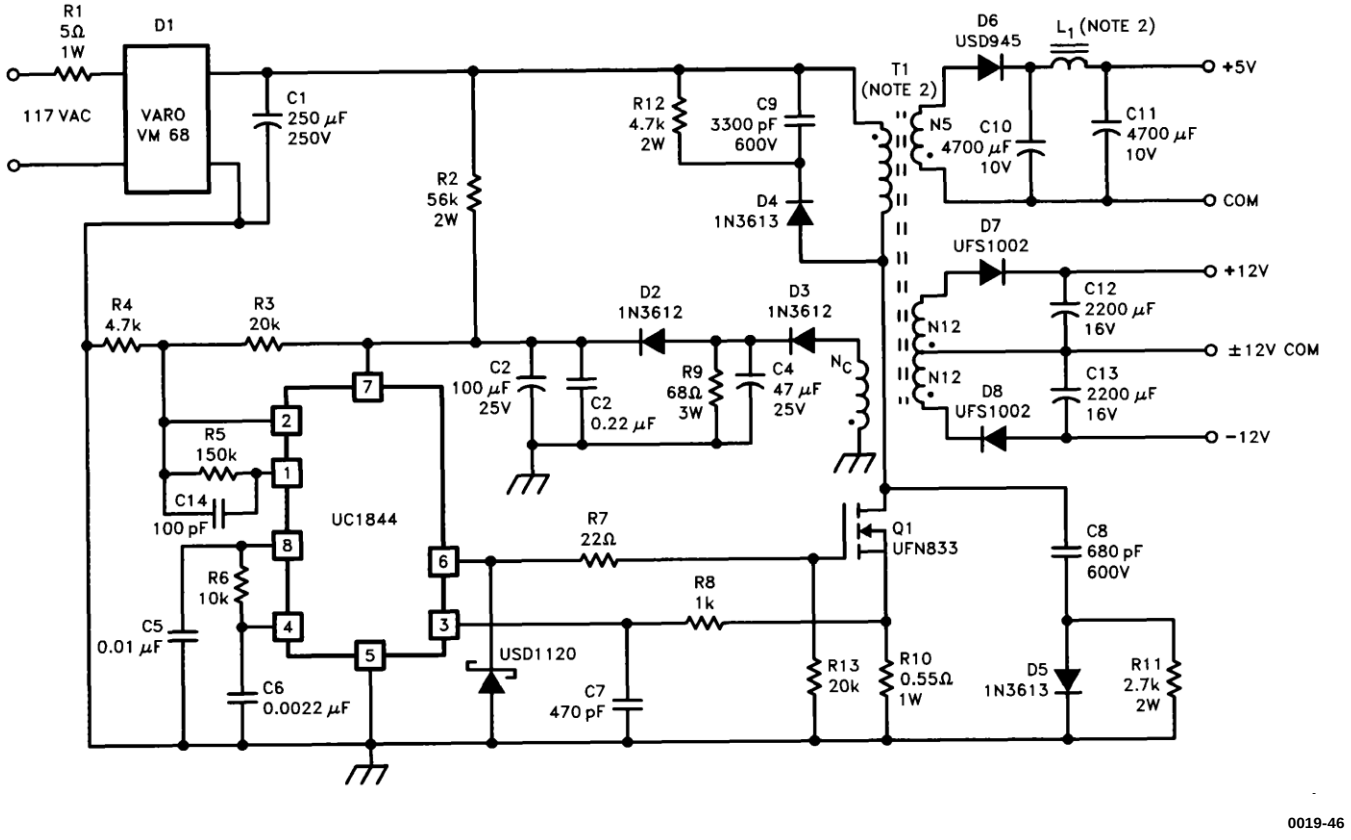

Figure 31

Power Supply Specifications

1. Input Voltage: 95 VAC to 130 VAC (50 Hz/60 Hz)
2. Line Isolation: 3750V
3. Switching Frequency: 40 kHz
4. Efficiency @ Full Load: 70%
5. Output Voltage:
   A. + 5V, ± 5%: 1A to 4A load
   Ripple voltage: 50 mV P-P Max.
   6. +12V, ±3% 0.1A to 0.3A load
   Ripple voltage: 100 mV P-P Max.
   C. -12V ±3%, 0.1A to 0.3A load
   Ripple voltage: 100 mV P-P Max.

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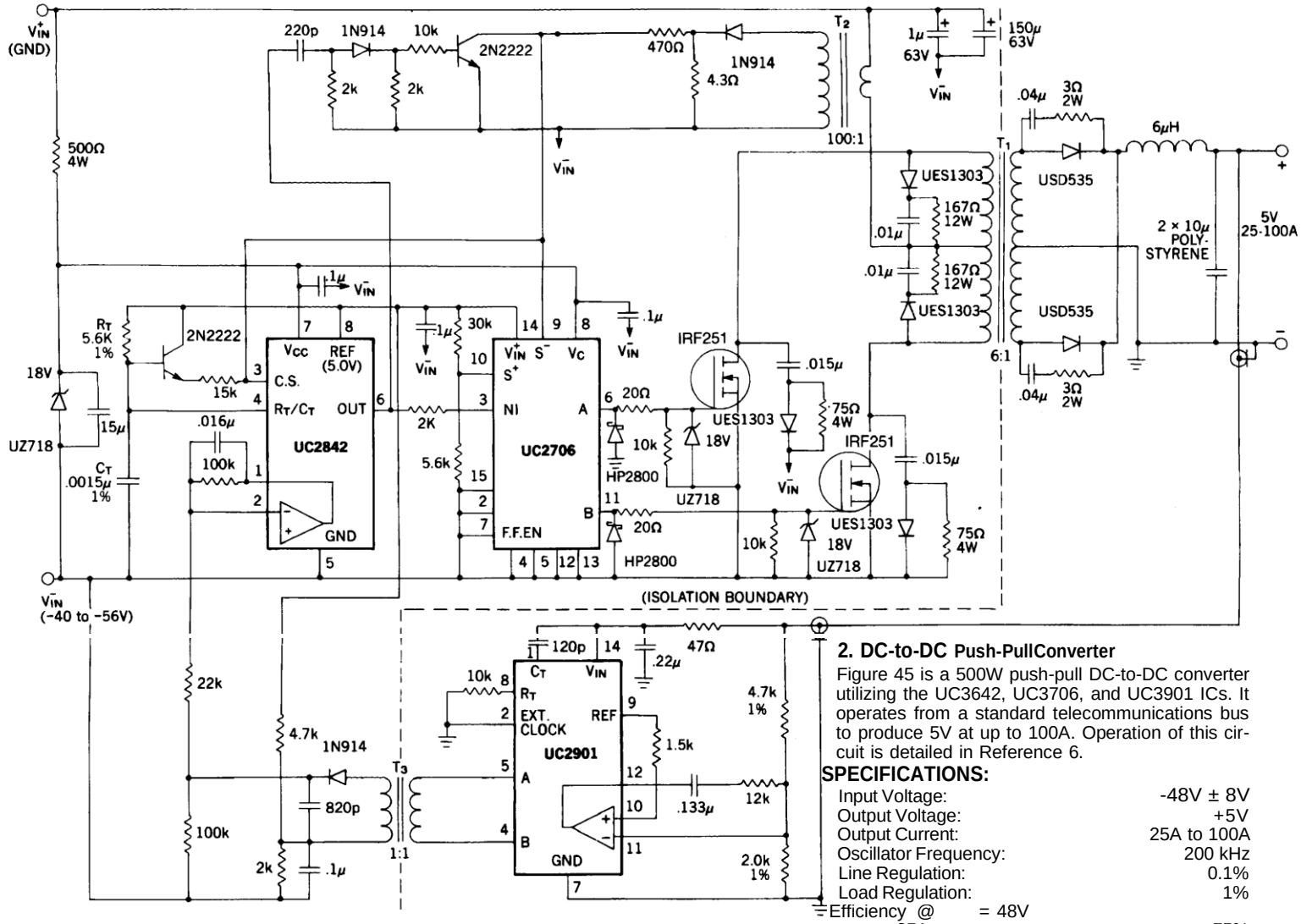

Figure 32. 500W Push-Pull DC-to-DC Converter

2. DC-to-DC Push-PullConverter

Figure 45 is a 500W push-pull DC-to-DC converter utilizing the UC3642, UC3706, and UC3901 ICs. It operates from a standard telecommunications bus to produce 5V at up to 100A. Operation of this circuit is detailed in Reference 6.

SPECIFICATIONS:

Input Voltage:	-48V ± 8V
Output Voltage:	+5V
Output Current:	25A to 100A
Oscillator Frequency:	200 kHz
Line Regulation:	0.1%
Load Regulation:	1%
Efficiency @ = 48V	
= 25A:	75%
= 50A:	80%
Output Ripple Voltage:	200 mV P-P

Also consult application note U-101 in the Unitrode Applications Handbook.

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